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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/590,796	06/08/2000	Gordon J. Vreugdenhil	1467-14	9846

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EXAMINER
SHARON, AYAL I

ART UNIT	PAPER NUMBER
2123	

DATE MAILED: 07/09/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/590,796	VREUGDENHIL ET AL.	
	Examiner	Art Unit	
	Ayal I Sharon	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 June 2000* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a)☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Introduction

1. Claims 1-23 of U.S. Application 09/590,796 filed on 06/08/2000 are presented for examination.

Claim Interpretations

2. Applicants define "slot" as follows (p.2, "Summary of the Invention"): "The simulator assembles a system of simultaneous equations. Equations that do not change depending on the circumstances are permanently associated with a system variable or slot. The conditions that apply to the conditional equations are evaluated. A conditional equation is active when the conditions related to the conditional equation evaluate to true. The active conditional equations are then assigned to slots in the system of simultaneous equations, which can then be solved to determine the values of the system variables." (Emphasis added).
3. Examiner interprets this functionality as being equivalent to the "simultaneous statements" functionality taught in the following 4 references:
    - IEEE Std 1076.1-1999. March 18, 1999. (pp.134-140, Section "9.5 Concurrent Signal Assignment Statements").

- Christen, E. et al. "VHDL 1076.1 – Analog and Mixed-Signal Extensions to VHDL". Proceedings EURO-DAC '96. Sept. 20, 1996. pp.556-561. (Section "3.3 Simultaneous Statements").
- Damon, D. et al. "Introduction to VHDL-AMS. 1. Structural and Discrete Time Concepts." Proc. 1996 IEEE Int'l Symposium on Computer-Aided Control System Design. Sept. 18, 1996. pp.264-269 (p.268, Section "2 VHDL Fundamentals – Simultaneous Equations").
- Christen, E. et al. "Introduction to VHDL-AMS. 2. Continuous and Mixed Continuous/Discrete Concepts." Proc. 1996 IEEE Int'l Symposium on Computer-Aided Control System Design. Sept. 18, 1996. pp.270-275 (p.271, Section "2 Differential / Algebraic Equations – Simultaneous Statements").

Claim Rejections - 35 USC § 112

1. The following is a quotation of the first paragraph of 35 U.S.C. 112:

   The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

2. Claims 1-23 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. The elements "selection

software", "assignment software", "solution software" and their equivalent methods have not been enabled in the specification.

3. Claims 22-23 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. The element "translation software" has not been enabled in the specification.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

5. The prior art used for these rejections is as follows:
6. IEEE Std 1076.1-1999. March 18, 1999. (Henceforth referred to as "**IEEE**").
7. The claim rejections are hereby summarized for Applicant's convenience. The detailed rejections follow.
8. **Claims 1-23 are rejected under 35 U.S.C. 102(a) as being clearly anticipated by IEEE.**
9. In regards to Claim 1, Christien teaches the following limitations:

1. In a computer simulation of a physical circuit or system including an analog or mixed signal digital-analog component, the physical circuit or system described in a hardware description language and characterized by a system of simultaneous equations, the method comprising:

representing the physical circuit or system as a system of simultaneous equations, the system of simultaneous equations including a slot for an active conditional equation and a dynamic slot target variable associated with the slot in the system of simultaneous equations;
(IEEE, especially: pp.134-140, Section "9.5 Concurrent Signal Assignment Statements")

selecting an active conditional equation at a current analog solution iteration;
(IEEE, especially: pp.134-140, Section "9.5 Concurrent Signal Assignment Statements")

assigning a value for the active conditional equation to a dynamic slot target variable at the current analog solution iteration, thereby associating the conditional equation with a slot in the system of simultaneous equations;
(IEEE, especially: pp.134-140, Section "9.5 Concurrent Signal Assignment Statements")

solving the system of simultaneous equations; and
(IEEE, especially: pp.134-140, Section "9.5 Concurrent Signal Assignment Statements")

using the solution to the system of simultaneous equations to validate the physical circuit or system.
(IEEE, especially: pp.134-140, Section "9.5 Concurrent Signal Assignment Statements")

10. In regards to Claim 2, Christien teaches the following limitations:

2. A method for solving a system of simultaneous equations including one or more conditional equations, the system of simultaneous equations describing a physical circuit or system in a hardware description language, the circuit including an analog component, the method comprising:

representing the physical circuit or system as a system of simultaneous equations, the system of simultaneous equations including one or more slots for active conditional equations selected from a set of possible characteristic expressions and one or more dynamic slot target variables associated with the slots in the system of simultaneous equations;
(IEEE, especially: pp.134-140, Section "9.5 Concurrent Signal Assignment Statements")

selecting a set of active conditional equations at a current analog solution iteration;
(IEEE, especially: pp.134-140, Section "9.5 Concurrent Signal Assignment Statements")

assigning a value for each active conditional equation in the set of active conditional equations to a dynamic slot target variable at the current analog solution iteration, thereby associating the active conditional equation with a slot in the system of simultaneous

equations; and
(IEEE, especially: pp.134-140, Section "9.5 Concurrent Signal Assignment Statements")

solving the system of simultaneous equations at the current analog solution iteration.
(IEEE, especially: pp.134-140, Section "9.5 Concurrent Signal Assignment Statements")

11. In regards to Claim 3, Christien teaches the following limitations:

3. A method according to claim 2, the method further comprising:

selecting a second set of active conditional equations at a second current analog solution iteration;
(IEEE, especially: pp.134-140, Section "9.5 Concurrent Signal Assignment Statements")

assigning a value for each active conditional equation in the second set of active conditional equations to a dynamic slot target variable at the second current analog solution iteration, thereby associating the active conditional equation with a slot in the system of simultaneous equations; and
(IEEE, especially: pp.134-140, Section "9.5 Concurrent Signal Assignment Statements")

solving the system of simultaneous equations at the second current analog solution iteration.
(IEEE, especially: pp.134-140, Section "9.5 Concurrent Signal Assignment Statements")

12. In regards to Claim 4, Christien teaches the following limitations:

4. A method according to claim 2, wherein assigning a value for each active conditional equation includes relating a system variable to each active conditional equation for the current analog solution iteration.
(IEEE, especially: pp.134-140, Section "9.5 Concurrent Signal Assignment Statements")

13. In regards to Claim 5, Christien teaches the following limitations:

5. A method according to claim 4, wherein solving the system of simultaneous equations includes determining a value for each system variable related to an active conditional equation.
(IEEE, especially: pp.134-140, Section "9.5 Concurrent Signal Assignment Statements")

14. In regards to Claim 6, Christien teaches the following limitations:

6. A method according to claim 2, wherein at most one conditional equation is assigned to each dynamic slot target variable at the current analog solution iteration.

(IEEE, especially: pp.134-140, Section "9.5 Concurrent Signal Assignment Statements")

15. In regards to Claim 7, Christien teaches the following limitations:

7. A method according to claim 2, wherein each conditional equation is assigned to at most one dynamic slot target variable at the current analog solution iteration.
(IEEE, especially: pp.134-140, Section "9.5 Concurrent Signal Assignment Statements")

16. In regards to Claim 8, Christien teaches the following limitations:

8. A method according to claim 2, wherein the number of active conditional equations is required to be equal to the number of dynamic slot target variables.
(IEEE, especially: pp.134-140, Section "9.5 Concurrent Signal Assignment Statements")

17. In regards to Claim 9, Christien teaches the following limitations:

9. A method according to claim 8, the method further comprising reporting a simulation failure if the number of active conditional equations differs from the number of dynamic slot target variables while attempting to solve the system of simultaneous equations.
(IEEE, especially: pp.134-140, Section "9.5 Concurrent Signal Assignment Statements")

18. In regards to Claim 10, Christien teaches the following limitations:

10. A method according to claim 2, wherein selecting an active conditional equation includes evaluating a condition associated with the active conditional equation.
(IEEE, especially: pp.134-140, Section "9.5 Concurrent Signal Assignment Statements")

19. In regards to Claim 11, Christien teaches the following limitations:

11. A method according to claim 10, wherein evaluating a condition occurs before selecting the active conditional equation.
(IEEE, especially: pp.134-140, Section "9.5 Concurrent Signal Assignment Statements")

20. Claims 12-21 are rejected based on the same reasoning as claims 2-11 above. Claims 12-21 are apparatus claims reciting the equivalent limitations as are recited in method claims 2-11 and taught throughout Chang et al.

21. In regards to Claim 22, Christien teaches the following limitations:

22. An apparatus for simulating a circuit, solving a system of simultaneous equations including a conditional equation, the system of simultaneous equations describing a physical circuit or system in a hardware description language, the circuit including an analog component, the apparatus comprising:

a computer for simulating the physical circuit or system;
(IEEE, especially: pp.134-140, Section "9.5 Concurrent Signal Assignment Statements")

a hardware description language description of the physical circuit or system stored on a computer-readable medium;
(IEEE, especially: pp.134-140, Section "9.5 Concurrent Signal Assignment Statements")

translation software to translate the hardware description language description into a system of simultaneous equations, the system of simultaneous equations including one or more slots for conditional equations selected from a set of possible conditional equations;
(IEEE, especially: pp.134-140, Section "9.5 Concurrent Signal Assignment Statements")

means for selecting a set of active conditional equations;
(IEEE, especially: pp.134-140, Section "9.5 Concurrent Signal Assignment Statements")

means for assigning a value for each active conditional equation in the set of active conditional equations to a dynamic slot target variable at the current analog solution iteration, thereby associating the active conditional equation with a slot in the system of simultaneous equations; and
(IEEE, especially: pp.134-140, Section "9.5 Concurrent Signal Assignment Statements")

means for solving the system of simultaneous equations at the current analog solution iteration.
(IEEE, especially: pp.134-140, Section "9.5 Concurrent Signal Assignment Statements")

22. In regards to Claim 23, Christien teaches the following limitations:

23. An apparatus according to claim 22, wherein the means for selecting an active conditional equation includes means for testing a condition associated with the active conditional equation.
(IEEE, especially: pp.134-140, Section "9.5 Concurrent Signal Assignment Statements")

Conclusion

23. The following prior art, made of record and not relied upon, is considered pertinent to applicant's disclosure.

24. Christen, E. et al. "VHDL-AMS – A Hardware Description Language for Analog and Mixed-Signal Applications". IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing. Vol. 46, Issue 10, Oct. 1999. pp.1263-1272. (See p.1263, col.2, second para., which teaches that this article is dedicated to teaching VHDL 1076-1993 and VHDL 1076.1-1999.)

25. Christen, E. et al. "VHDL 1076.1 – Analog and Mixed-Signal Extensions to VHDL". Proceedings EURO-DAC '96. Sept. 20, 1996. pp.556-561. (See Section "3.3 Simultaneous Statements").

26. Damon, D. et al. "Introduction to VHDL-AMS. 1. Structural and Discrete Time Concepts." Proc. 1996 IEEE Int'l Symposium on Computer-Aided Control System Design. Sept. 18, 1996. pp.264-269 (See p.268, Section "2 VHDL Fundamentals – Simultaneous Equations").

27. Christen, E. et al. "Introduction to VHDL-AMS. 2. Continuous and Mixed Continuous/Discrete Concepts." Proc. 1996 IEEE Int'l Symposium on Computer-Aided Control System Design. Sept. 18, 1996. pp.270-275 (See p.271, Section "2 Differential / Algebraic Equations – Simultaneous Statements").

28. Shi, R. "VHDL-A: Analog Extension to VHDL". Proc. 7th Annual IEEE Int'l ASIC Conf. and Exhibit, 1994. Sept. 23, 1994. pp.160-165.

29. Saleh, et al. "Analog Hardware Description Languages". Proc. of IEEE 1994 Custom Integrated Circuits Conf. May 4, 1994. pp.349-356.

30. Mantooth, H.A. et al. "Beyond Spice with Saber and MAST". 1992 IEEE Int'l Symposium on Circuits and Systems (ISCAS '92). May 13, 1992. vol.1, pp.77-80.

31. Vlach, M. "Modeling and Simulation with Saber". Proc., 3rd Annual IEEE ASIC Seminar and Exhibit, 1990. Sept. 21, 1990. pp.T/11.1-T/1111.

32. Vlach, J. "Computer Oriented Formulation of Equations and Analysis of Switch-Capacitor Networks". IEEE Transactions on Circuits and Systems. Vol.31, Issue 9, Sept. 1994. pp.753-765.

33. Christen et al., U.S. Patent 6,532,569.

34. Mantooth et al., U.S. Patent 6,236,956.

35. Vlatch et al. U.S. Patent 5,548,539.

36. Vlatch, U.S. Patent 4,985,860.

37. Smith et al., U.S. Patent 4,868,770.

Correspondence Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ayal I. Sharon whose telephone number is (703) 306-0297. The examiner can normally be reached on Monday through Thursday, and the first Friday of a biweek, 8:30 am – 5:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kevin Teska can be reached on (703) 305-9704. Any response to this office action should be mailed to:

Director of Patents and Trademarks
Washington, DC 20231

Hand-delivered responses should be brought to the following office:

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The fax phone numbers for the organization where this application or proceeding is assigned are:

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Non-Official / Draft communications	(703) 746-7240
After Final communications	(703) 746-7238

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist, whose telephone number is: (703) 305-3900.

Ayal I. Sharon

Art Unit 2123

June 29, 2003

KEVIN J. TESKA
SUPERVISORY
PATENT EXAMINER